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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/796,426	03/09/2004	Brian Robert Prasky	POU920030068US1	1895

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EXAMINER
JOHNSON, BRIAN P

ART UNIT	PAPER NUMBER
2183	

MAIL DATE	DELIVERY MODE
10/16/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

	Application No.	Applicant(s)
Office Action Summary	10/796,426	PRASKY ET AL.
	Examiner	Art Unit	
	Brian P. Johnson	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☒ Responsive to communication(s) filed on *31 July 2007*.

2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.

3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) ☒ Claim(s) *1,4,8-14,19-28,30,31,34,38-41 and 46-50* is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5) ☐ Claim(s) _____ is/are allowed.

6) ☒ Claim(s) <u>*1, 4, 8, 9-14, 19-28, 30, 31, 34, 38-41, and 46-50*</u> is/are rejected.

7) ☐ Claim(s) _____ is/are objected to.

8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) ☐ The specification is objected to by the Examiner.

10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a) ☐ All b) ☐ Some * c) ☐ None of:

      1. ☐ Certified copies of the priority documents have been received.

      2. ☐ Certified copies of the priority documents have been received in Application No. _____.

      3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☐ Information Disclosure Statement(s) (PTO/SB/08)
    Paper No(s)/Mail Date _____.

4) ☐ Interview Summary (PTO-413)
    Paper No(s)/Mail Date. _____.

5) ☐ Notice of Informal Patent Application

6) ☐ Other: _____.

DETAILED ACTION

1.   Claims 1, 4, 8, 9-14, 19-28, 30, 31, 34, 38-41, and 46-50 are pending.

Papers Filed

2.   Examiner acknowledges receipt of amendments and remarks filed 9 March 2004

October 2006 and subsequent corrections.

Non-compliant Claim Objections

1.   Examiner notes that despite the multiple notices of non-compliance that have

been sent the claims are still non-compliant. In particular:

Claim 4: triple brackets are used for deletion rather than the required double

brackets. An unnecessary strike out is used as well. Several other claims contain the

same error.

Claims 19, 20: not only are triple brackets used for deletion, but also one set of

the triple brackets have been stricken out.

Claim 38: a partial strike out of the space immediately subsequent to the "28" is

used for an unknown purpose.

Claim 46: Applicant has reintroduced the exact same problem that was

discussed in a non-compliant action mailed 07 March 2007 and temporarily filed on 16

March 2007 and 09 April 2007 version of the claims.

Examiner urges Applicant to review MEPE 1.121

Title

3.   Objection is withdrawn.

Specification

4.   Objections are withdrawn.

Claim Objections

5.   It appears that Applicant intended to cancel claims 25 and 26. They relate to the

same basis as cancelled claims 2 and 3 and their limitations are included in

independent claim 24.

Claim Rejections - 35 USC § 101

6.   Rejection is withdrawn.

Claim Rejections - 35 USC § 103

7.   The following is a quotation of 35 U.S.C. 103(a) which forms the basis for

all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set
> forth in section 102 of this title, if the differences between the subject matter sought to be patented and
> the prior art are such that the subject matter as a whole would have been obvious at the time the
> invention was made to a person having ordinary skill in the art to which said subject matter pertains.
> Patentability shall not be negatived by the manner in which the invention was made.

1.   Claims 1, 4, 8-13, 19-28, 30, 31, 34, 38-40, and 46-50 are rejected under 35

U.S.C. 103(a) as being unpatentable over Stiles et al. (U.S. Patent No. 6,425,075).

8.   As per claim 1, Stiles teaches a method of operating a computer having a

pipelined processor having a branch target buffer (BTB) (Fig. 2 cache 155) comprising

creating a recent entry queue (Fig. 2 cache 152) said recent entry queue comprising a

set of branch target buffer (BTB) entries (col 3 lines 28-38) in parallel with the branch

target buffer (BTB), organizing the recent entry queue as a FIFO queue (col 10 lines 37-

40), comparing an entry to be written into the BTB against valid entries within the recent

entry queue (col 10 lines 41-67), searching the recent entry queue to detect looping

branches (col 9 lines 35-37) comparing the branch to determine if it was recently written

into the queue (col 10 lines 37-40), determining if the branch is backwards branching

whereby a looping branch is detected (col 3 lines 28-38), and if a looping branch is

detected that is not predicted thereafter delaying a decode (col 7 lines 7-12), and writing

an entry into the BTB when it is also written into the recent entry queue (col 9 lines 22-

34).

9.   Stiles fails to disclose it comprising blocking an entry matching an entry within the

recent entry queue from being written into the BTB.

10.   Official Notice is taken that arranging the caches in a tiered arrangement (like a

typical L1-L2 cache setup) is well known in the art. A tiered arrangement of cache

levels allows the system to write an entry into only the L1 cache rather than spending

the time and resources to write into both the L1 and L2. Upon eviction from the L1

cache, the entry is written into the L2. The examiner asserts that with this arrangement,

any entry (including those that match current entries in the L1) will be blocked from

writing to the L2 cache.

It would have been obvious to one of ordinary skill in the art at the time of
invention to have arranged Stiles' caches in a tiered L1-L2 arrangement for the benefit
of conserving system resources on writing an entry to the BTB.

11.   As per claim 4, Stiles teaches the method of claim 3 wherein the recent entry
queue is full[y] associative for reading. (Col. 3 lines 63-64)

12.   As per claim 8, Stiles teaches the method of claim 1 comprising searching the
BTB for a next predicted branch and evaluating the recent entry queue while the BTB is
being indexed. (Col. 9 lines 35-37)

13.   As per claim 9, Stiles teaches the method of claim 8 wherein the recent entry
queue maintains a depth up to the associatively of the BTB whereby while the BTB is
indexed, the recent entry queue positions are input to comparison logic. *The examiner
asserts that the L1 BPC maintains a depth of as many entries as possible, as dictated
by the LRU replacement algorithm (col. 10 lines 37-40). Further, since the L2 BPC is
disclosed as being direct mapped, (col. 16 line 7) it has an associatively of 1. The L1
BPC has been disclosed as having a depth greater than 1.*

14.   As per claim 10, Stiles teaches the method of claim 8 comprising searching the
recent entry queue [for] a matching branch in parallel to searching BTB output. (Col. 9
lines 35-37)

15.   As per claim 11, Stiles teaches the method of claim 10 comprising creating hit

detect logic to support the associatively of the BTB. (Col. 16 lines 10-20)

16.   As per claim 12, Stiles teaches the method of claim 8 comprising using a subset

of the recent entry queue as a subset of the BTB. *The examiner asserts that since an*

branch data entry can be indexed into both the L1 and L2 BPC, the entries in the L1

BPC constitute a subset of those in the L2.

17.   As per claim 13, Stiles teaches the method of claim 12 comprising fast indexing

recently encountered branches. *The examiner asserts that since the L1 BPC holds*

fewer entries, it inherently can be checked for a pending branch more quickly than the

L2 BPC, which stores many more entries.

18.   As per claim 19, Stiles teaches the method of claim 18 comprising delaying

decode until a fixed number of cycles. *The decode is inherently delayed by the number*

of clock cycles it takes to flush the pipeline.

19.   As per claim 20, Stiles teaches the method of claim 19 comprising delaying

decode until the BTB predicts a branch. *Inherently, the branch target instruction will not*

be decoded until it has been predicted to have been taken.

20.   As per claim 21, Stiles teaches the method of claim 1 comprising staging writes

to the BTB in the recent entry queue. *The examiner asserts that BTB writes are stored*

in the L1 BPC (Col. 3 lines 27-38)

21.   As per claim 22, Stiles teaches the method of claim 21 [comprising] delaying a

write and placing the write in the recent event queue. *The examiner asserts that a write*

to the BTB is delayed until the first iteration of the branch has been evaluated for target

address and direction. · Since the L1 BPC stores this information (col. 3 lines 48-55) it is

not possible to place the data in the BPC until it has been calculated.

22.   As per claim 23, Stiles teaches the method of claim 22 [comprising] detecting a

predicted branch while its BTB write is temporarily staged in the recent entry queue.

(Col. 3 lines 28-38)

23.   Claim 24 is directed toward a computer implementing the method of claim 1 and

is rejected under the same grounds as stated above.

24.   As per claim 26, Stiles teaches the method of claim 1 wherein the recent entry

queue comprises a set of branch target buffer (BTB) entries. (Col. 3 lines 28-38)

2.   As per claim 27, Stiles teaches the method of claim 2 comprising organizing the

recent entry queue as a FIFO queue. (Col. 10 lines 37-40) *The examiner asserts that*

Stiles' invention removes entries from the L1 BPC in the order in which they were

accessed. The first to be accessed are the first to be removed.

25.   Claim 27 is directed toward a computer implementing the method of claim 4 and

is rejected under the same grounds as stated above.

26.   Claims 28, 31, 34, 38-40, and 46-50 are directed toward a program product

implementing the method of claims 1, 4 9-13, and 19-23, respectively, and are rejected

under the same grounds as stated above.

27.   Claims 14 and 41 are rejected under 35 U.S.C. 103(a) as being unpatentable

over Stiles.

28.   As per claim 14, Stiles teaches the method of claim 12 but fails to teach it

[comprising] searching the complete recent entry queue to block duplicate BTB writes.

29.   Official Notice is taken that updating an existing entry in a cache is well known in

the art. Checking for an existing entry eliminates the wasting of memory space for a

pending store which matches an entry already in the cache.

30.   It would have been obvious to one of ordinary skill in the art at the time of

invention to have checked the L1 BPC for an existing entry before writing into a new

position for the benefit of not wasting memory space.

31.   Claim 41 is directed toward a program product implementing the method of claim

14 and is rejected under the same grounds as stated above.

Response to Arguments

3.   Applicant's arguments filed 31 July 2007 have been fully considered but they are

not persuasive.

4.   Applicant quotes several claim citations that the cited references allegedly fail to

disclose; however, Applicant fails to make any particular arguments. The claims, as

amended, contain citations that show the disclosure of every element.

Conclusion

5.   **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time

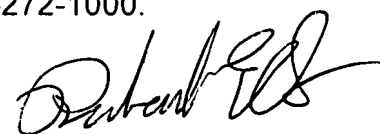policy as set forth in 37 CFR 1.136(a).

        A shortened statutory period for reply to this final action is set to expire THREE

MONTHS from the mailing date of this action. In the event a first reply is filed within

TWO MONTHS of the mailing date of this final action and the advisory action is not

mailed until after the end of the THREE-MONTH shortened statutory period, then the

shortened statutory period will expire on the date the advisory action is mailed, and any

extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later

than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the

examiner should be directed to Brian P. Johnson whose telephone number is (571) 272-

2678. The examiner can normally be reached on 8-4:30 M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's

supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for

the organization where this application or proceeding is assigned is 571-273-8300.

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system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

RICHARD L. ELLIS
PRIMARY EXAMINER